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Small-area low-power heart condition monitoring system using dual-mode SAR-ADC for low-cost wearable healthcare systems

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Abstract.
BACKGROUND: Heart rate monitoring is useful to detect many cardiovascular diseases. It can be implemented in a small device with low power consumption, and it can exploit low-cost piezoelectric pressure sensors to measure heart rate. However, it is also desirable to transmit heartbeat waveform for emergency treatment, which significantly increases transmission power.
OBJECTIVE: In this paper, a low-cost wireless heart condition monitoring SoC is proposed. It can monitor and transmit both heart rate and heartbeat waveform, but the hardware is extremely simplified to achieve in a small package.
METHODS: By slight modification of successive-approximation analog-digital converter, it can count heart rate and read out heartbeat waveform with the same hardware. In the normal mode, only an 8-bit heart rate is transmitted for power reduction. If the heart rate is out of a given range, it goes to the emergency mode and a 10-bit heartbeat waveform is transmitted for fast treatment.
RESULTS: The fabricated chip size is 1.1 mm^2 in 0.11 μm CMOS technology, including the radio-frequency transmitter. The measured power consumption is 161.8 μW in normal mode and 507.3 μW in emergency mode, respectively.
CONCLUSION: The proposed SoC achieves low-cost, small area, and low-power. It is useful as part of a disposable healthcare system.

Keywords: Heart rate monitoring, wearable healthcare system, SAR-ADC, dual-mode, low-power

1. Introduction

Recently, wearable healthcare system has become one of the most promising solutions for healthcare services with senior citizens. One of the major researches in this field is Electrocardiography (ECG) monitoring circuits [1–3]. However, they require expensive ECG sensors, complex readout integrated circuits (ROIC), large-area digital signal processors (DSP), and high-power radio-frequency transmitters (Tx) [4]. From these reasons, they are not suitable for low-cost wearable healthcare systems embedded in clothes.

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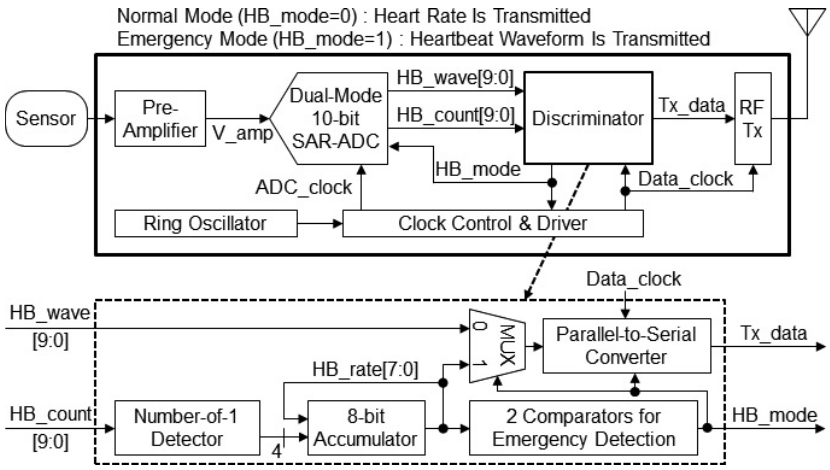

Fig. 1. Architecture of the proposed wireless heart condition monitoring SoC.

Heart rate monitoring is useful to detect many cardiovascular diseases such as heart attack, angina, myocardial infarction, coronary heart disease, congestive heart failure, and sleep apnea syndrome [5,6]. It can exploit low-cost piezoelectric pressure sensors [7], which enables disposable healthcare systems. It does not require large-area DSPs. In addition, its ROIC chip area and Tx power consumption are small because of large input signal and low bitrate. However, for emergency treatment, it is desirable to transmit detailed heartbeat waveform, which significantly increases Tx power consumption.

This paper proposes a small-area low-power wireless heart condition monitoring SoC. It only consists of a clock generator, a preamp, a successive-approximation analog-digital converter (SAR-ADC), a Tx, and small control logic. The preamp can read out 150 mV signal from a piezoelectric pressure sensor. The SAR-ADC can read out of 0.9 V signal with 10-bit resolution. It is modified to perform both heart rate counting and heartbeat waveform readout in the same hardware, where only 6 MUXes and half-VDD generator are added. The Tx performs on-off-keying (OOK) transmission with 0 dBm output power.

When the measured heart rate is within a given range, the device diagnoses that the person has no cardiovascular problems. Then, it operates in normal mode and transmits only heart rate in 8-bit resolution for Tx power reduction. Its Tx ON duty ratio is 2.7×10^{-5}%. When the measured heart rate is out of a given range, the device diagnoses that cardiovascular problem occurs. Then, it operates in emergency mode and transmits whole heartbeat waveform in 10-bit resolution for fast emergency treatment. Its Tx ON duty ratio is 1.94%. The fabricated chip size is 1.1 mm^2 in 0.11 μm CMOS technology. The measured power consumption is 161.8 μW in normal mode and 507.3 μW in emergency mode, respectively.

2. Proposed wireless heart condition monitoring system

The proposed wireless heart condition monitoring SoC is illustrated in Fig. 1.

2.1. Preamp

Commercial low-cost piezoelectric pressure sensor was used in the proposed heart condition monitoring system. It can measure heartbeat waveform with about 120 mV output range. Note that typical

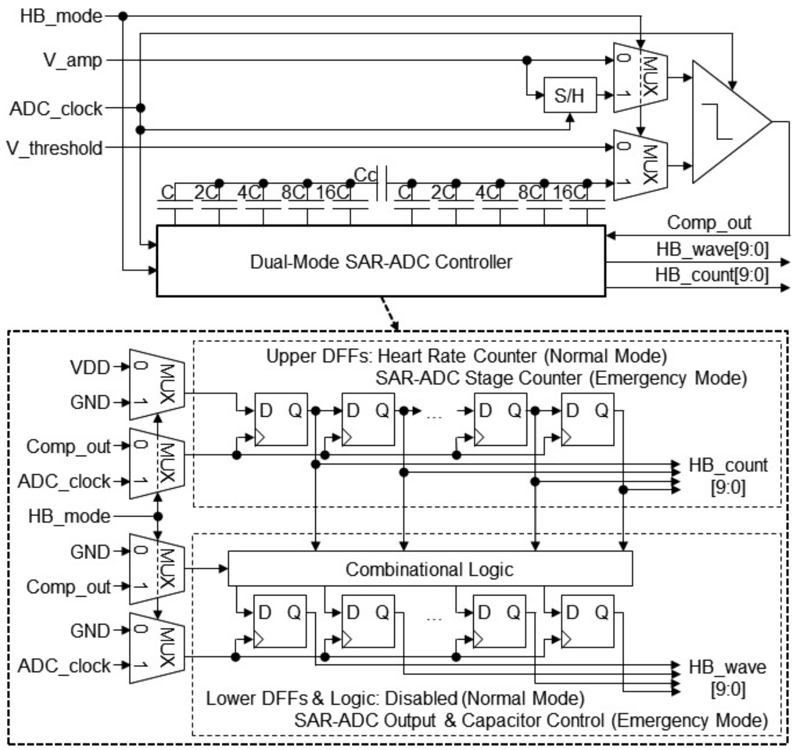

Fig. 2. The proposed dual-mode SAR-ADC.

input signal range of ECG sensors is several mV. Because the output voltage of the piezoelectric pressure sensors is much larger than that of the ECG sensors, the preamp can be implemented with simple and small circuit. The preamp consists of a 2-stage operational amplifier, registers, and capacitors. It amplifies input signal with a gain of 6. It filters input noise with −3 dB cut-off frequency of 1 kHz. Its input and output voltage range is 150 mV and 0.9 V, respectively.

2.2. SAR-ADC

The proposed 10-bit dual-mode SAR-ADC is illustrated in Fig. 2. It performs both heart rate counting and heartbeat waveform readout. In order to select appropriate signals for each mode, only 6 MUXes are added. Half VDD generator is also added to make reference voltage for heartbeat pulse detection. In the conventional 10-bit SAR-ADC, 20 D flip-flops (DFF) control SAR-ADC stages and capacitors, and store waveform data. In the proposed dual-mode SAR-ADC, these DFFs also count and store heart rate data.

2.2.1. Normal mode operation

In normal mode ($HB\_mode = 0$, $ADC\_clock = 60$ Hz), switched capacitors are disabled, and the dual-mode SAR-ADC operates as a heart rate counter. Upper 10 DFFs run as a modified asynchronous ripple counter. Lower 10 DFFs and its logic are disabled. It counts the rising edges of heartbeat pulse during 4 seconds (= 240 *ADC_clock* cycles). The heartbeat pulse count is then transferred to the discriminator, and the dual-mode SAR-ADC starts to count the heartbeat pulses for the next 4 seconds. Note that the discriminator counts the heart rate during 1 minute, so the discriminator period accumulates 15 values of SAR-ADC heartbeat pulse counts. Its detailed operation is described as the pseudocodes in Fig. 3.

```
V_threshold is generated as half VDD;
lower 10 DFFs and its logic are disabled by setting their inputs to GND;
for every 240 ADC_clock cycles {
  upper 10 DFFs are cleared;
  for every ADC_clock cycle {
    Comp_out detects the crossing of V_amp across V_threshold;
    Comp_out is fed into the clock of upper 10 DFFs;
    positive edge of Comp_out increases HB_count[9:0] along the sequence of

     (1000000000)→(1100000000)→(1110000000)→(1111000000)…;

    if (240th ADC_clock cycle is reached)
      break;
  }
  HB_count[9:0] are transferred to discriminator;
}
```

Fig. 3. Pseudocodes of normal mode operation.

2.2.2. *Emergency mode operation*

In emergency mode (*HB_mode* = 1, *ADC_clock* = 15 kHz), the dual-mode SAR-ADC operates as a conventional 10-bit SAR-ADC. The upper 10 DFFs operates as a synchronous ring counter, which indicates what stage is being executed. The lower 10 DFFs and its logic control the switched capacitors. The dual-mode SAR-ADC takes 15 *ADC_clock* cycles (= 1 ms) to read 1 sample of heartbeat waveform, so its sampling frequency is 1 kHz.

2.3. *Discriminator*

The discriminator calculates heart rate from SAD-ADC output and decides operation mode. It also performs parallel-to-serial conversion to make *Tx_data*. The number of 1's in *HB_count*[9:0] is recorded by simple combination logic, and these values are accumulated in 15 times to calculate *HB_rate*[7:0] (= heart rate during 1 minute). Operation mode is decided by checking whether heart rate is within normal range (48∼96 pulses/minute). The operation mode and the threshold range of normal heart rate can be externally set for application purpose.

2.4. *Tx*

Tx has 1 on-chip inductor, and it performs 1-channel OOK transmission with 0 dBm output power. It can sufficiently transmit data to about 10 m, which is a typical distance for wearable healthcare systems with in-room receivers. Tx bitrate is 620 kbps, so *Data_clock* = 620 kHz.

Figure 4 illustrates the Tx timing diagram. Tx transmits few fixed-length data bits periodically. The rest of the time, Tx is turned OFF for power reduction. In normal mode, heart rate is transmitted once within a minute. It requires 10-bit transmission, i.e. 1-bit *start code*, 1-bit *HB_mode*, and 8-bit *HB_rate*. Tx ON duty ratio is 10 bit/(620 kbps $*$ 60 s) = $2.7 \times 10^{-5}\%$, so the Tx power in normal mode is almost negligible.

While in emergency mode, heartbeat waveform is transmitted once in a millisecond. It requires 12-bit transmission, i.e. 1-bit *start code*, 1-bit *HB_mode*, and 10-bit *HB_wave*. Tx ON duty ratio is

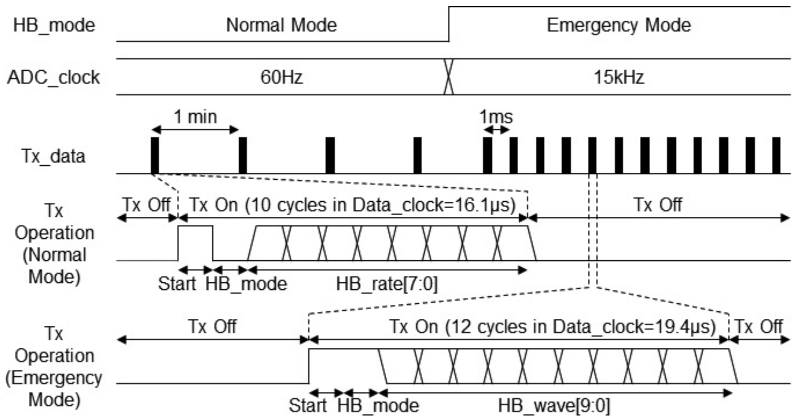

Fig. 4. Tx timing diagram of the proposed wireless heart condition monitoring SoC.

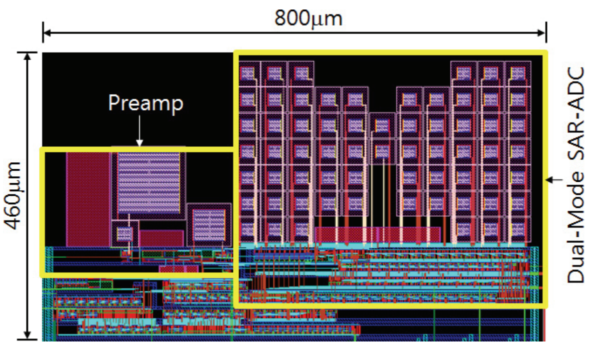

Fig. 5. Layout of the ROIC/control.

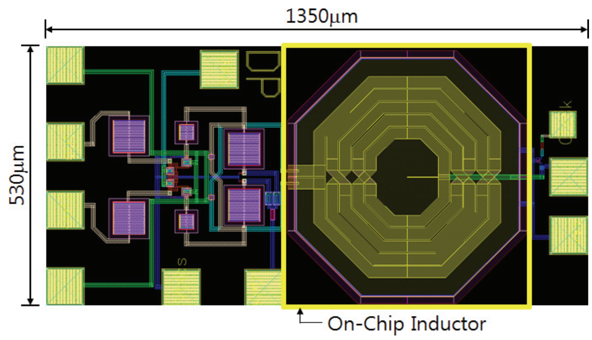

Fig. 6. Layout of the Tx.

12 bit/(620 kbps $*$ 1 ms) $=$ 1.94%. Emergency mode consumes much more power compared to when it is in normal mode, which can cause the battery to be exhausted after a long period of being on emergency mode operation. However, it is enough to save a life by one-time emergency detection/treatment for disposable low-cost wearable healthcare system.

3. Implementation, measurement, and evaluation

The proposed wireless heart condition monitoring SoC is implemented and fabricated in 0.11 μm CMOS technology. Figure 5 shows the layout of the monitoring circuit including a dual-mode SAR-ADC and a preamp. Figure 6 shows the layout of the Tx including an on-chip inductor. Total chip area is 1.09 mm^2, which is significantly small. VDD is 1 V for both ROIC and Tx.

The fabricated chip is mounted on the test board for functional verification and power measurement, as shown in Fig. 7. Off-the-shelf piezoelectric pressure sensor is mounted on the wrist rubber band, and it is connected to the test board by wire. Figure 8 shows the measured heartbeat waveform by the piezoelectric pressure sensor. Figure 9 shows the measurement results of the preamp and the SAR-ADC. 50 mV peak-to-peak sinusoidal test input signal is applied to the preamp. The preamp and the SAR-ADC can successfully measure the input signal, and the output binary codes of the SAR-ADC are almost the same compared with the input signal.

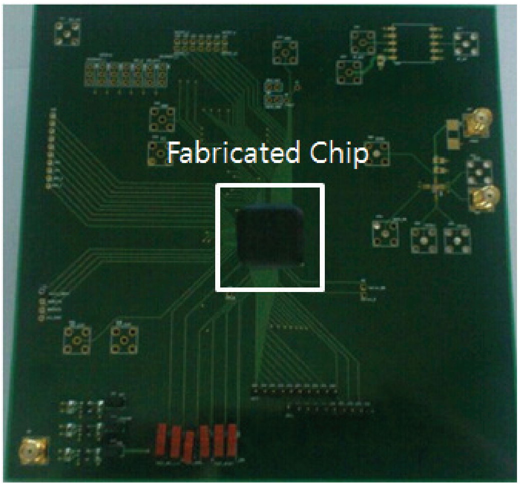

Fig. 7. The test board.

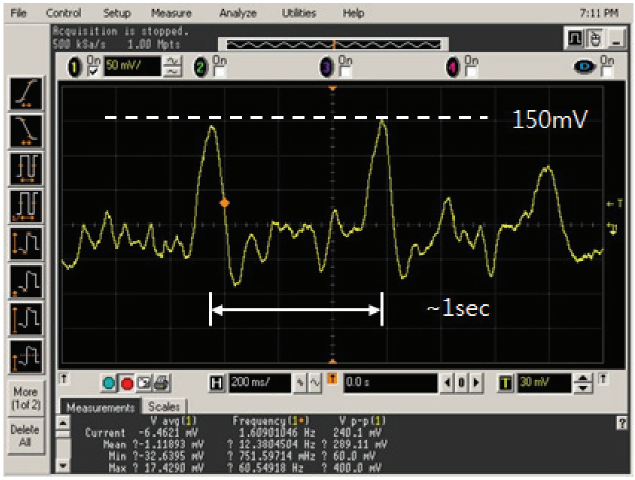

Fig. 8. Measured heartbeat waveform by the piezoelectric sensor.

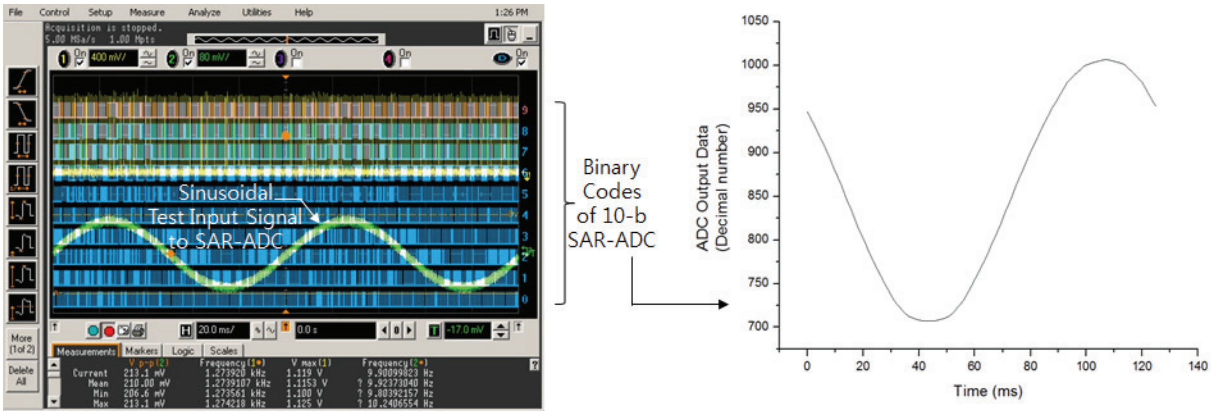

Fig. 9. Measurement results of the preamp and the SAR-ADC.

Table 1 shows the implementation and measurement results. Its power consumption is 161.8 μW in normal mode and 507.3 μW in emergency mode.

Table 2 shows the performance comparison with previous researches [1–3]. [1] achieved small area, but it is a 3-chip solution and it does not have control logic. In addition, its power consumption is much larger with lower Tx output power. [2] achieved 16 channels and additional functions such as thoracic impedance variance [8,9], but its power consumption and area are too large. [3] achieved low power consumption and additional functions such as bio-impedance [10], but its area is too large. In addition, it does not have Tx.

Based on the comparison, the proposed SoC shows quite good cost-performance. In addition, it can exploit low-cost piezoelectric pressure sensor. This can reduce the inconvenience of patch-type ECG sensors. The architecture of the proposed SoC is extremely simple, and it can be applied to many low-cost healthcare applications. From above, the proposed SoC can significantly reduce the manufacturing cost of the equipment, and it can achieve low-cost disposable wearable healthcare systems that can be embedded in the clothes.

Table 1
Implementation and measurement results

Terms		Results	
		Normal mode	Emergency mode
Chip area	ROIC/control	0.37 mm^2	
	Tx	0.72 mm^2	
	Total	1.09 mm^2	
Operation frequency	ADC_clock	60 Hz	15 kHz
	Data_clock	620 kHz	
VDD		1 V	
Tx bitrate		620 kbps	
Tx ON duty ratio		2.7×10^{-5}%	1.94%
Tx transmission period		60 s	10^{-3} s
Tx transmission interval length		16.1 μs	19.4 μs
Simulated maximumpower consumption	Preamp	4.8 μW	4.8 μW
	SAR-ADC	140 μW	209 μW
	Clock generator	181 μW	181 μW
	Digital/control	2 μW	2 μW
	Tx	0.004 μW	290.3 μW
	Total	327.8 μW	687.1 μW
Measured average power consumption[1]		161.8 μW	507.3 μW

[1]Simulated maximum Tx current is 15 mA. Tx power in each mode is calculated based on its duty ratio.

Table 2
Performance comparison

Terms	Performance			
	Ref. [1]	Ref. [2]	Ref. [3]	Proposed
Fabrication technology	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.11 μm CMOS
Chip area	1.19 mm^2	25 mm^2	25 mm^2	1.09 mm^2
Power consumption	8.9×10^3 μW	3.9×10^3 μW	56.16 μW	161.8 μW/507.3 μW
Tx output power	−1.72 dBm	−75 dBm	No Tx	0 dBm
Functions	ECG	ECG + thoracic impedance variance + data compression	ECG + feature extraction + bio-impedance	Heart rate + heartbeat waveform + emergency detection
Number of channels	2	16	3	1
Signal monitoring	△ (No control logic)	O	O	O
Tx unit	△ (No control logic)	O	X	O
Rx unit	X	O	X	X
Integration	3 Chips (No control logic)	1 Chip	1 Chip	1 Chip

4. Conclusions

In this paper, a low-cost wireless heart condition monitoring SoC is proposed to measure and transmit heart rate and heartbeat waveform. It also detects emergency state by monitoring heart rate. It has extremely simplified hardware architecture. The proposed dual-mode SAR-ADC can monitor heart rate and heartbeat waveform with negligible additional hardware. When it is in the normal mode, only the heart rate is transmitted for power reduction. If the heart rate is out of a given range, it goes to the emergency mode and whole heartbeat waveform is transmitted for fast treatment. In addition, it can exploit low-cost piezoelectric pressure sensors. The proposed SoC was implemented in 0.11 μm CMOS technology. The proposed SoC is suitable for low-cost wearable healthcare systems.

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