Guest-editorial

Low-power embedded systems

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Historically, digital systems have been designed with performance and area in mind. Other cost functions such as testability and energy consumption were mainly regarded as side constraints to be used in the design phase. It was only in the early 90's that the role of power consumption changed from that of a design constraint to an actual design metric.

The main driving factor for this trend is the exploding market of portable electronic appliances, which calls for complex integrated systems that can be powered by lightweight batteries with long times between recharges.

A coarse classification of modern electronic products separates general-purpose systems (i.e., systems that are able to perform a variety of different tasks and that contain very powerful and highly-flexible programmable processors) from embedded systems (i.e., systems that are devoted to very specific functions, whose architectures and implementations are optimized for the target application).

As the integration capabilities offered by modern technologies increase, it is now quite common finding devices that offer simultaneously a large variety of functions and services: Image and video processing, sound processing, data and voice communication. System operation is user-driven by means of simple programming, and tasks are carried out by a processor-based architecture (possibly containing more than one embedded core processor) implemented within a single chip.

Purpose of this special issue is that of introducing the readers with advanced techniques and methods for the design of low-power embedded systems. The main source of material for the issue is the 2003 edition of PATMOS, the International Workshop on Power &

Timing Modeling, Optimization and Simulation. After a thorough process of peer review, which involved over 30 experts in the field, 8 papers were selected for publication.

The first paper of this issue addresses the problem of the efficient exploration of the architectural design space for parameterized microprocessor-based systems.

In the second paper, a new method for creating instruction level energy models for pipelined processors is introduced.

The third paper presents a new tool for power estimation of caches built inside a unified framework for the design of embedded systems.

The fourth paper describes an algorithm to explore, for an application or a set of applications, the loop buffer design space in order to reduce the energy consumption in the instruction memory hierarchy of an embedded processor.

The fifth paper describes a new design methodology for implementing multimedia applications with reduced power consumption.

In the sixth paper, a systematic approach of data clustering and calculation scheduling aiming at minimal memory requirements in wavelet-based signal coders is proposed.

The seventh paper presents a new power management technique aimed at increasing the energy efficiency of client-server multimedia applications running on wireless portable devices.

Finally, the last paper describes a scalable, highly parallel architecture for UMTS compliant Turbo decoding and an architecture-driven voltage scaling is applied to reduce the energy consumption.

All the submissions to the special issue were of extremely valuable quality, and I thus thank all the contributors for their effort. I hope that the readers will appreciate the papers I have selected, and I hope that this issue will serve as a stimulus for opening up new research investigations in the area of low-power embedded systems.

Alberto Macii
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