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## The Fifth Special Issue on Application of Concurrency to System Design

## Preface

This fifth special issue of Fundamenta Informaticae presents revised versions of papers presented at the 6th International Conference on Application of Concurrency to System Design (ACSD). The ACSD conference series serves as a forum for disseminating theoretical results, advanced methods and tools for the design of complex concurrent systems. The extent of the topics addressed contributes to cross-fertilisation:

- Methods for the design of synchronous or asynchronous systems based on models of concurrency (data-flow, communicating automata, Petri nets, process algebras, statecharts, MSCs etc.),
- synchronous and asynchronous systems,
- scheduling of embedded systems,
- hardware synthesis,
- timed and stochastic systems specification and analysis,
- efficient algorithms for verification of concurrent systems,
- application of formal verification to mobile networks and systems-on-chips,
- semantics and algebraic approaches.

The articles of this issue have been selected from the sixth ACSD conference, held in Turku, Finland, 28–30 June, 2006. The conference proceedings, published by the IEEE Computer Society, contain 23 contributions, each with a length of about 10 pages. The acceptance rate was 50 %. Moreover, the proceedings contain 3 papers describing tools demonstrated during the conference. We have selected five of the papers presented at the conference for this special issue. The selection was based on the reviews of the conference program committee and their presentation during the conference. The authors were asked to compile a complete journal presentation from their conference papers. These papers have been revised after additional rounds of reviewing.

The papers presented in this issue cover various fields from the ACSD topics. However, this selection can be considered representative for the discussion at the ACSD conference.

The order of contributions is alphabetical w.r.t. the last name of the first author.

In the first paper, Javier Esparza, Petr Jančar and Alexander Miller address two key problems in the domain of asynchronous circuits specification. Such systems are modelled using Signal Transition Graphs (STGs), for which consistency and completeness should be guaranteed. Algorithms are exhibited, leading to important complexity results, for a subclass of STGs, namely marked graph STGs.

The second paper, by Gabriel Juhás, Robert Lorenz and Sebastian Mauser, presents a stratified-order structure based approach for defining causality semantics for Petri nets. This causality semantics captures and distinguishes "earlier than" and "not later than" causalities between events, in addition to the usual "independence". The results obtained are applied to the class of elementary nets with inhibitor arcs, equipped with the *a priori* semantics.

Resolution of encoding conflicts on STGs is addressed in the third paper, written by Victor Khomenko, Agnes Madalinski and Alex Yakovlev. The framework is based on the construction and analysis of prefixes of the net unfolding. Two techniques allow for solving conflicts: concurrency reduction and signal insertion. The validity of the transfomations applied guarantees properties preservation.

In the fourth paper, schedulabity issues are tackled by Cong Liu, Alex Kondratyev, Yosinori Watanabe and Jörg Desel. This is a relevant problem for industrial applications. The paper exhibits two sufficient conditions for unschedulabiblity, based on structural properties of the Petri net modelling the system under study. Therefore the schedulability problem can be investigated efficiently. The approach is assessed by its application to small industrial examples.

Finally, the fitfh paper, authored by Tiberiu Seceleanu and Axel Jantsch, deals with heterogeneous real-time embedded systems, which has both synchronous and asynchronous components. A formal specification is used to devise a correct-by-construction transformation of the system model. The asynchronous interactions with the environment are dealt with, using a *watched variables* mechanism. This is applied to a symple audio processing system case study.

We appreciate the work of all authors and we are grateful to all reviewers for their useful criticism.

Ryszard Janicki Department of Computing and Software McMaster University Hamilton, Ontario, Canada L8S 4K1 janicki@cas.mcmaster.ca Laure Petrucci LIPN, CNRS UMR 7030 Université Paris 13 99, avenue Jean-Baptiste Clément 93430 Villetaneuse, France Laure.Petrucci@lipn.univ-paris13.fr

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