

The Fourth Special Issue on Applications of Concurrency to System Design

Preface

This is the fourth special issue of *Fundamenta Informaticae* with revised versions of papers presented at the International Conference on Application of Concurrency to System Design (ACSD). The ACSD conference series serves as a forum for disseminating theoretical results, advanced methods and tools for the design of complex concurrent systems. In particular, it aims at cross-fertilizing both types of research on the following topics:

- Methods for the design of synchronous or asynchronous systems based on models of concurrency (data-flow, communicating automata, Petri nets, process algebras, statecharts, MSCs etc.),
- correct-by-construction design methods and integration of verification techniques with the design process,
- synchronous/asynchronous design and communication interfaces: Globally Asynchronous Locally Synchronous systems,
- hardware/software co-design from common specifications,
- concurrency issues in Systems on Chips (use of formal methods for communication protocol design and verification).

The articles of this issue have been selected from the fifth ACSD conference, held in St. Malo, France, 7-9 June, 2005. These conference proceedings, published by the IEEE Computer Society, contain 26 contributions, each with a length of about 10 pages. The acceptance rate was 50 %. We have selected six of the papers presented at the conference for this special issue. The selection was based on the reviews of the conference program committee. The authors were asked to compile a complete journal presentation from their conference papers. These papers have been revised after reviews from three experts for each paper.

The papers presented in this issue cover various fields from the ACSD topics. However, this selection can be considered representative for the discussion at the ACSD conference.

The order of contributions is alphabetical w.r.t. the last name of the first author.

In the first article Robert Clarisó and Jordi Cortadella present a technique for the generation of gate-level timing constraints in asynchronous circuits. The time bounds are either given by constants or by parameters. The main contribution is an innovative representation of the parametric timed state space based on bit-vectors. The authors present the results of experiments showing that the kind of linear constraints that appear when analyzing timed circuits are more efficiently represented using octahedra than convex polyhedra. This way, verification is significantly more efficient with a small impact on the accuracy of the derived constraints.

The second article, authored by Marc Geilen, Twan Basten, Bart Theelen and Ralph Otten, introduces a novel, algebraic approach to Pareto analysis which is particularly designed to allow for describing incremental design decisions and composing sets of Pareto-optimal configurations. The introduced algebra of Pareto points is illustrated with a case-study on transmitting an MPEG-4 video stream delivery chain from a server to a hand-held device.

The automated synthesis of Asynchronous data Communication Mechanisms (ACMs) is the topic of the third article. The authors are Kyller Gorgôni, Jordi Cortadella, Fei Xia and Alex Yakovlev. The work advances previous ACM synthesis methods by algorithms which automate most of the synthesis process. It makes use of a particular Petri net class and of the theory of regions. The practicality of the introduced method is illustrated by means of a 4-cell OWBB ACM, with a state graph with 1120 states and 2240 arcs.

The fourth article, authored by Mark Josephs and Hemangee Kapoor, considers delay-insensitive processes, specified with the so-called DI-Algebra. This algebra is based on CSP. The contribution relates DI-Algebra to an alternative theory of delay-insensitive processes (developed by Verhoeff) which is based on a testing paradigm and the concept of reflection. Controllability of processes in DI-Algebra is introduced and the algebra is extended by a reflection operator. The final contribution is a modified version of Verhoeff's factorisation theorem.

In the fifth article Dumitru Potop-Butucaru and Benoît Caillaud introduce a new model for the representation of asynchronous implementations of synchronous specifications. This model covers both, classical implementations with global synchronization being preserved by signaling, and globally asynchronous, locally synchronous (GALS) implementations without global clock. The model is used to derive criteria ensuring the correct deployment of synchronous specifications over GALS architectures (w.r.t. semantics preservation and deadlock absence preservation).

Finally the sixth article, written by Walter Vogler and Ben Kangsah, builds on previous approaches for the specification of asynchronous circuit behaviour by Signal Transition Graphs (STGs), a variant of Petri nets. For coping with complex specifications, the decomposition of a specification is necessary. This work extends previously defined decomposition techniques.

We appreciate the work of all authors and we are grateful to all reviewers for their useful criticism.

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