

Special Issue on Application of Concurrency to System Design

Preface

The articles in this special issue of *Fundamenta Informaticae* are revised versions of selected papers presented in the Fourth International Conference on Application of Concurrency to System Design (ACSD'04) held in Hamilton, Ontario, Canada, 16-18 June, 2004. The first conference in the series was held in Aizu-Wakamatsu, Japan, March 1998, the second in Newcastle upon Tyne, U.K., June 2001, the third in Guimarães, Portugal, June 2003. The journal versions of six selected papers from ACSD'01 were published in *Fundamenta Informaticae*, Vol. 50, Number 2, April 2002, and the journal versions of five selected papers from ACSD'03 were published in *Fundamenta Informaticae*, Vol. 62, Number 2, July 2004.

The seven papers have been chosen from 21 contributions accepted for presentation at ACSD'04, following their additional evaluation and editorial treatment.

Like its predecessors, the Hamilton Conference was organized to provide a forum for disseminating advanced research results on theory, algorithms, and case studies arising in the design of concurrent systems.

The chosen articles cover asynchronous circuits, reactive systems, model checking, process algebras, refinement, verification and synthesis problems. The order of contributions is alphabetical.

The first article, by D. Björklud and J. Lilius, is an interesting exercise in formal development of a language for multiple models of computation. It shows, how the programs represented as abstract syntax trees, can automatically be translated into B specifications. The paper uses B-Method in an unorthodox way.

In the second article, H. K. Kapoor, M. B. Josephs and D. P. Furey show how delay insensitive circuits can be formally synthesized in a way that takes their environment into account, resulting in more efficient implementation. The formal operators of the delay insensitive process algebra are studied and reduced to special cases of synchronization. Relationships between the operators used to take the environment into consideration are studied.

The third article, by V. Khomenko, M. Koutny and A. Yakovlev, addresses the problem of logic synthesis for asynchronous circuits described as signal transition graphs (STGs). To avoid constructing the

reachability graph of an STG, which often leads to state explosion, the authors use only the information about causality and structural conflicts between the events involved in a finite and complete prefix of its unfolding. An efficient algorithm for logic synthesis based on the Incremental Boolean Satisfiability (SAT) is proposed. This article was given *the best conference paper award*.

The fourth article, by M. Lawford, V. Pantelic and H. Zhang, describes an attempt to combine theorem proving and model-checking to formally verify real-time systems in a discrete time setting. The time automata modelling environment has been modified to provide a formal model for time transition models in the PVS proof checker.

In the fifth article, K. Seppi, M. Jones and P. Lamborn, proposes a new meta-heuristic for use in finding errors in models of complex concurrent systems using explicit guided model checking. The meta-heuristic improves explicit guided model checking by applying the empirical Bayes method to revise heuristic estimates of the distance from a given state to an error.

In the sixth article, H. Tauriainen generalizes the classic explicit-state emptiness checking algorithm for Büchi word automata into Büchi automata with multiple acceptance conditions.

The seventh and last article, by F. Xia, F. Hao, I. Clark, A. Yakovlev and E. Graeme Chester, describes a systematic design/synthesis process for asynchronous communication mechanisms (ACMs) with arbitrary buffer size, a series of resulting buffered ACM algorithms, and the modelling and simulation of these ACMs using Matlab.

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