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Special issue on Application of Concurrency to System Design

The articles in this special issue of Fundamenta Informaticae are revised versions of selected papers presented in the Second International Conference on Application of Concurrency to System Design (ACSD'01) held in Newcastle upon Tyne,UK, 25-29 June, 2001. The first conference in the series was held in Aizu-Wakamatsu,Japan, March 1998. The papers have been chosen from 20 contributions accepted for presentation at ACSD'01, following their additional evaluation and editorial treatment.

Like its predecessor, the Newcastle Conference was organized to provide a forum for disseminating advanced research results on theory, algorithms, and case studies arising in the design of concurrent systems.

The chosen articles cover performance issues, asynchronous communication, asynchronous circuits, verification and testing, and synthesis problems. The order of contributions is alphabetical.

The first article by M. Baldamus and K. Schneider is devoted to the use of BDDs for program verification in a novel way by studying the size of BDDs used to represent the transition systems with shared variables. Interleaving, synchronous and asynchronous types of concurrency are considered.

In the second article, J. Carmona, J. Cortadella and E. Pastor address the problem of automation of control-dominated circuit synthesis from Signal Transition Graphs (STG) specification. A new approach to insertion of signal transition into STG to make the latter implementable is proposed.

In the third article, O. Garnica, J. Lancharos and R. Hermida, analyse the behaviour and performance of asynchronous pipelines, i.e., pipelines in which stages have logical clocks. Using a set of timing parameters characterizing the computing and communication delays of stages, a formula describing the performance of the pipeline is derived, and several specific pipeline configurations are discussed.

The fourth article by M. Pietkiewicz-Koutny addresses a characterization of the class of step transition systems generated by the concurrent execution of elementary net systems with inhibitor arcs under the a-posteriori semantics, and compares them with the class of step transition systems obtained under the a-priori semantics.

In the fifth article, F. Xia and I. Clark present new algorithms for the Signal and Message asynchronous data communication mechanism (ACM), and their modelling and analysis using Petri net techniques. The authors classify ACMs based on the possibility that a process accessing the ACM may overwrite or reread stored data.

The sixth and last article by W. Zuberek provides a performance analysis of multithreaded multiprocessor systems by mean of timed Petri nets. Four timed Petri net models, each one emphasizing a different aspect of the system, are discussed.

I am very grateful to the authors for submitting their papers and to the referees for their useful criticism.

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